CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor device comprising the steps of:

forming a gate dielectric layer on a semiconductor substrate;

forming a gate electrode over the gate dielectric layer wherein the gate electrode defines a channel interposed between source/drain regions formed within an active region of the semiconductor substrate; and

forming contact etch resistant spacers on sidewalls of the gate electrode and sidewalls of the gate dielectric layer,

the contact etch resistant spacers being of a non-silicon oxide and a non-nitride material.

2. The method according to claim 1, wherein the step of forming the contact etch resistant spacers includes the steps of:

forming a contact etch resistant layer on the sidewalls of the gate electrode, the sidewalls of the gate dielectric and portions of the upper surface of the semiconductor substrate; and

etching the contact etch resistant layer to form the contact etch resistant spacers.

3. The method of claim 2, further including the step of:

forming the contact etch resistant layer of at least one of silicon carbide and undoped silicon.

4. The method of claim 1, further including the step of:

forming a liner layer over the contact etch resistant spacers of at least one of Si_xN_y and SiO_xN_y.

5. The method of claim 1, further including the step of:

forming an interlevel dielectric layer over the contact etch resistant spacers of SiO_x.

6. The method of claim 5, further including the step of:

forming a contact mask over the interlevel dielectric layer; and

etching a contact aperture to expose a source/drain region.

7. A semiconductor device comprising:

a dielectric layer interposed between a gate electrode and a semiconductor substrate; and

contact etch resistant spacers formed on sidewalls of the dielectric layer and sidewalls of the gate electrode,

the contact etch resistant spacers being of a non-silicon oxide and a non-nitride material.

8. A semiconductor device according to claim 7, wherein the contact etch resistant spacers are at least one of silicon carbide and undoped silicon.

9. The semiconductor device according to claim 8, wherein the contact etch resistant spacer is silicon carbide.

10. The semiconductor device according to claim 8, wherein the contact etch resistant spacer is undoped silicon.

11. The semiconductor device according to claim 7, further including a liner layer formed over the contact etch resistant spacers, wherein the liner layer is at least one of Si_xN_y and SiO_xN_y.

12. The semiconductor device according to claim 7, further including an interlevel dielectric layer (ILD) formed over the contact etch resistant spacers, wherein the ILD layer is SiO_x.

13. A semiconductor device comprising:

a gate dielectric layer disposed over a semiconductor substrate;

a gate electrode formed on the gate dielectric layer defining a channel interposed between source/drain regions formed within an active region of the semiconductor substrate; and

contact etch resistant spacers formed on sidewalls of the dielectric layer and sidewalls of the gate electrode,

the contact etch resistant spacers being of a non-silicon oxide and a non-nitride material.

14. A semiconductor device according to claim 13, wherein the contact etch resistant spacer is at least one of silicon carbide and undoped silicon.

15. The semiconductor device according to claim 14, wherein the contact etch resistant spacer is silicon carbide.

16. The semiconductor device according to claim 14, wherein the contact etch resistant spacer is undoped silicon.

17. The semiconductor device according to claim 13, further including a liner layer formed over the contact resistant spacers, wherein the liner layer is at least one of Si_xN_y and SiO_xN_y.

18. The semiconductor device according to claim 17, wherein the liner layer is Si_xN_y.

19. The semiconductor device according to claim 17, wherein the liner layer is SiO_xN_y.

20. The semiconductor device according to claim 13, further including an interlevel dielectric layer (ILD) formed over the contact etch resistant spacers, wherein the ILD layer is SiO_x.